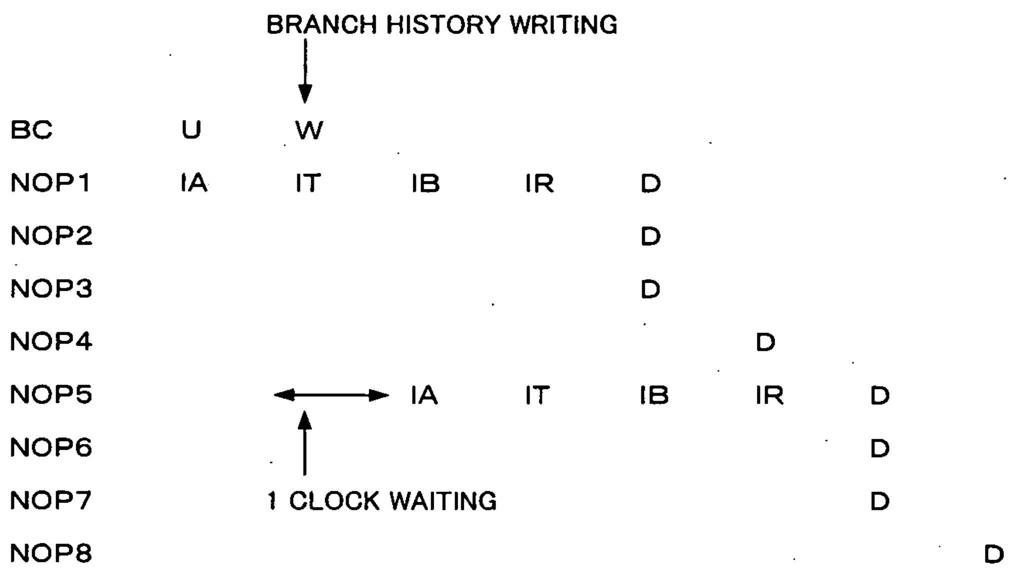


F I G. 1 Prior Art

EXAMPLE OF SHORT LOOP

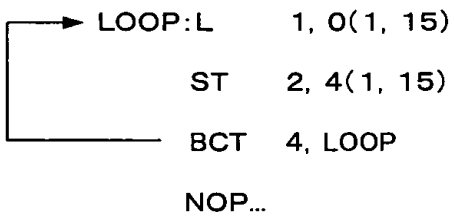


FIG. 2A Prior Art

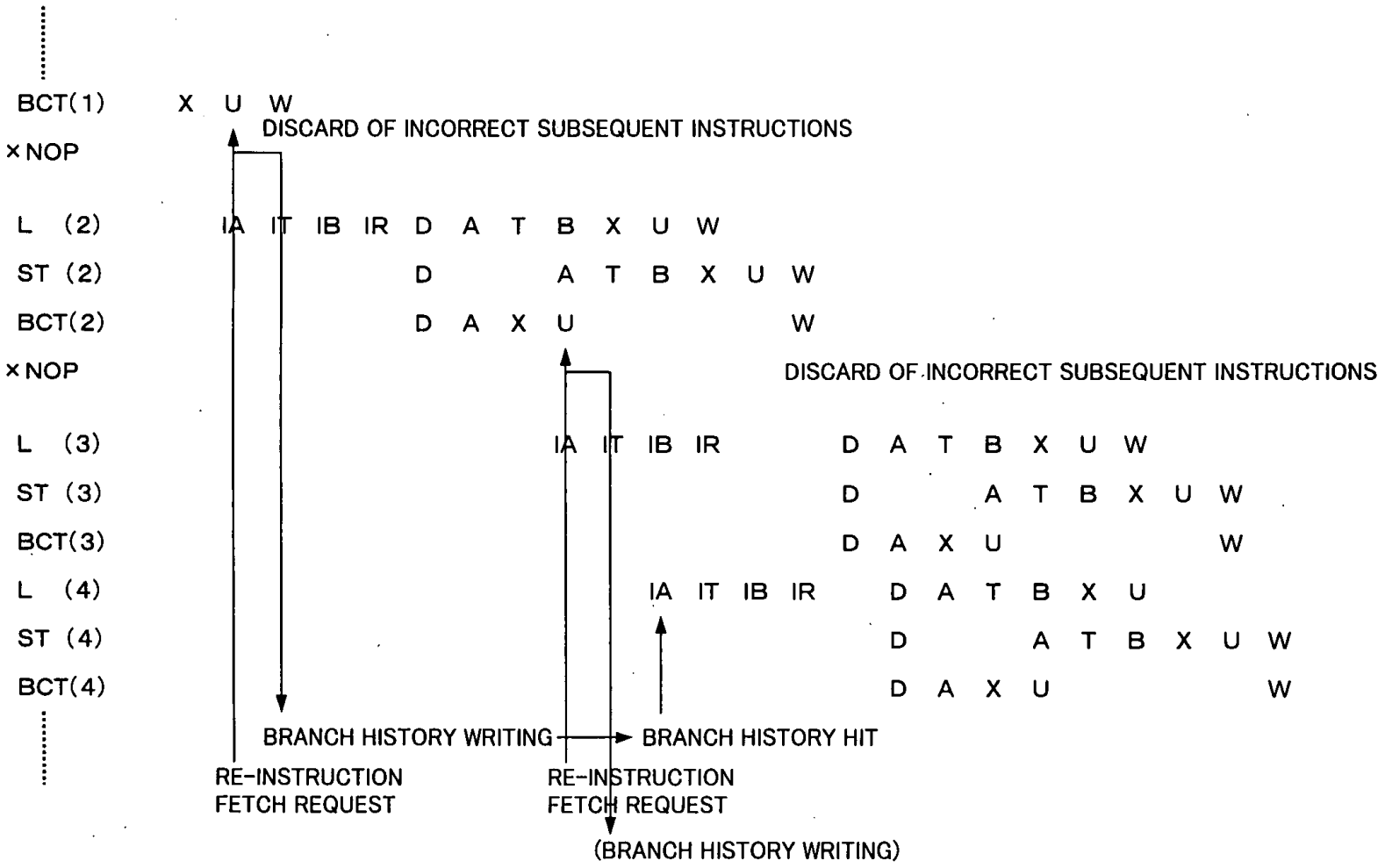


FIG. 2B Prior Art

BC	U	W					
NOP1	IA	IT	IB	IR	D		
NOP2					D		
NOP3					D		
NOP4						D	
NOP5		IA	IT	IB	IR	D	
NOP6						D	
NOP7							D
NOP8							D

IMPROVEMENT OF AVERAGE 1 CLOCK CYCLE

FIG. 3

EXAMPLE OF SHORT LOOP

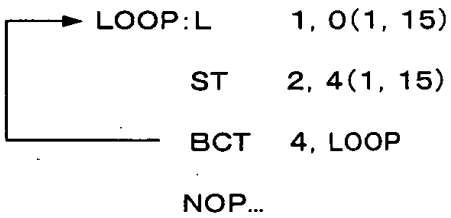


FIG. 4A

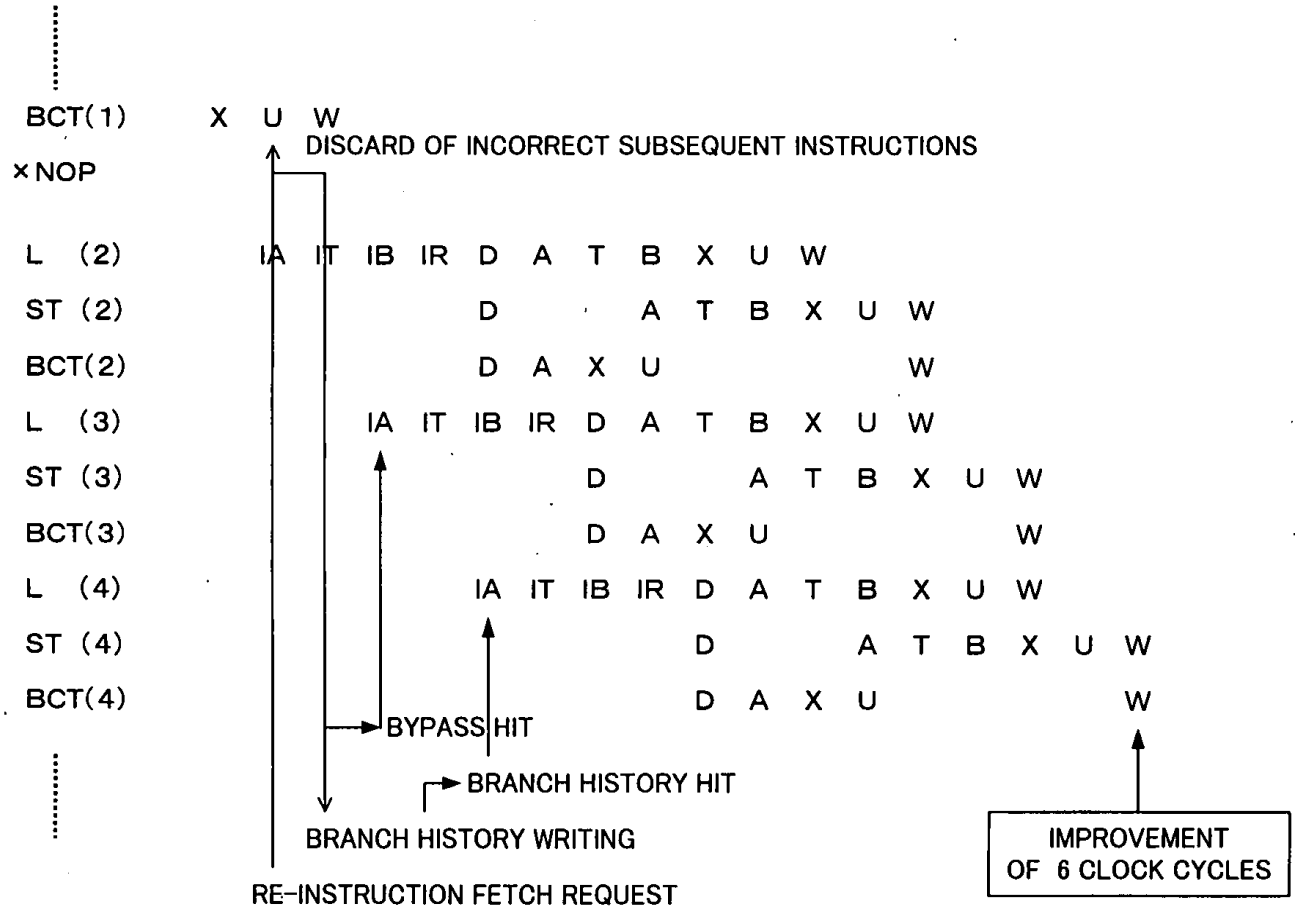


FIG. 4B

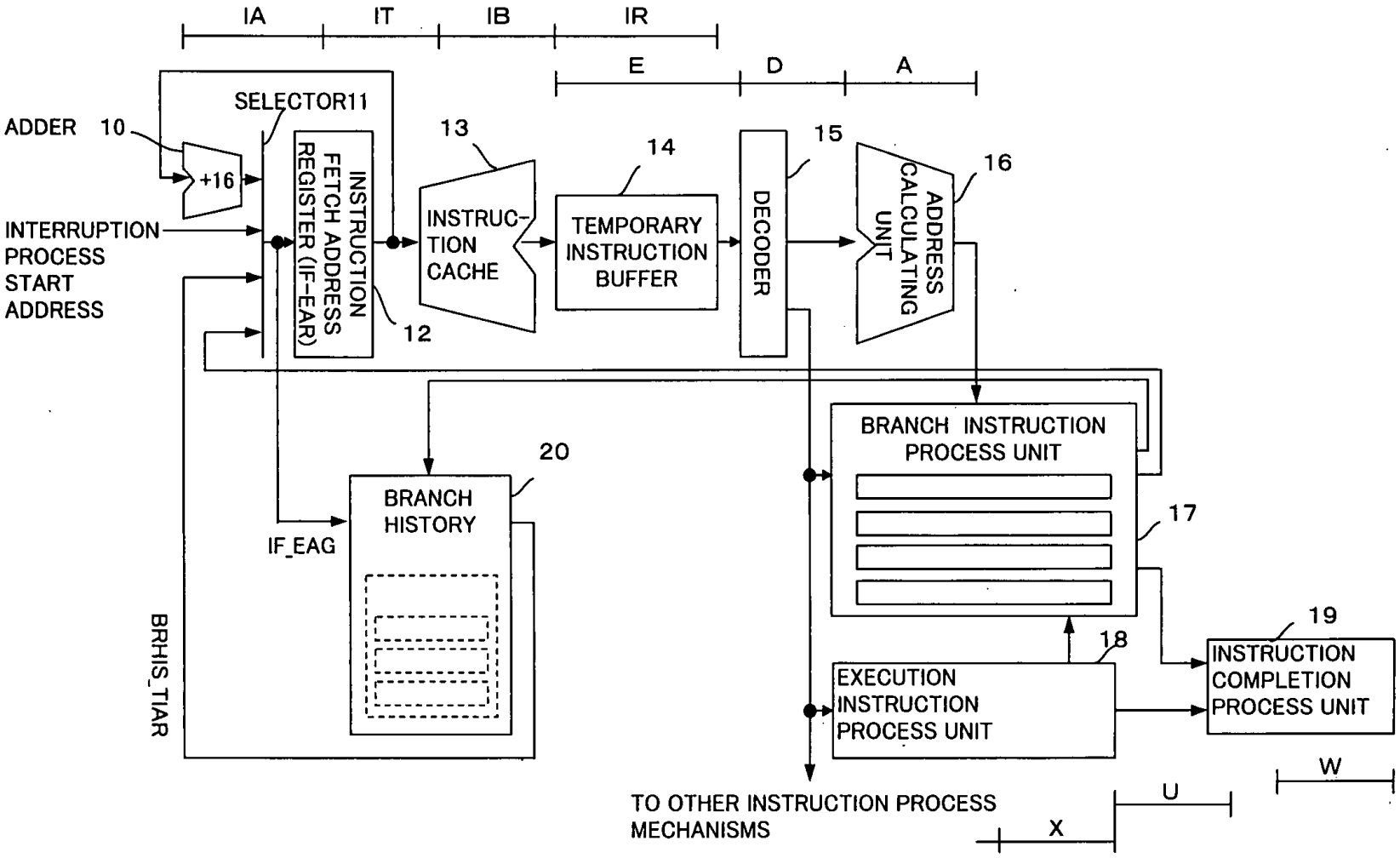
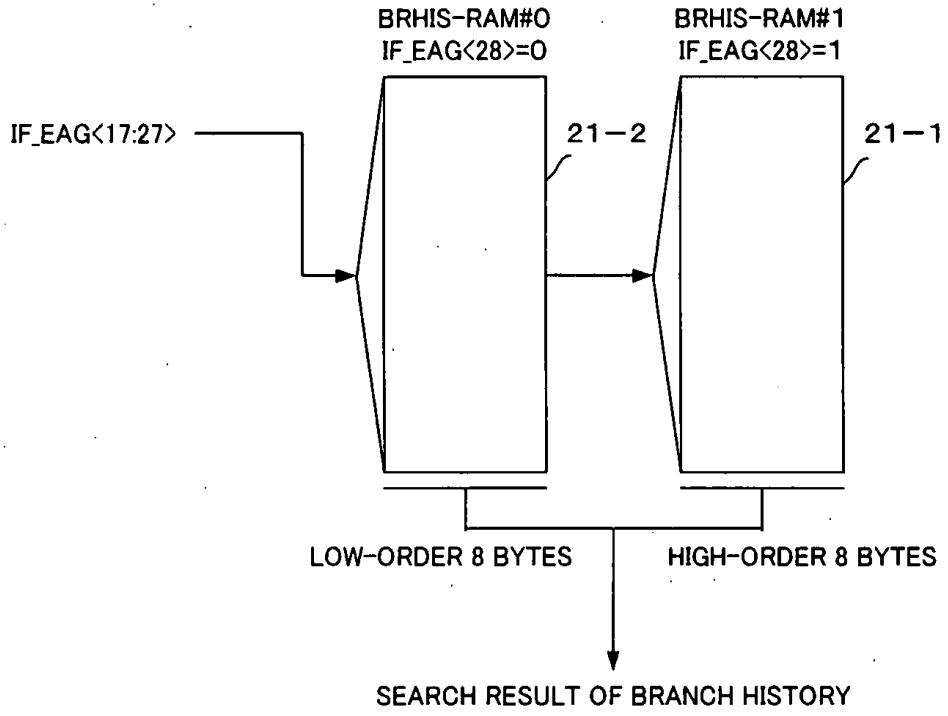

IA
IT
IB
IR
E
D
A
SELECTOR11
ADDER
10
+16
INTERRUPTION PROCESS START ADDRESS
INSTRUCTION FETCH ADDRESS REGISTER (IF-EAR)
12
13
INSTRUC-TION CACHE
14
TEMPORARY INSTRUCTION BUFFER
15
DECODER
16
ADDRESS CALCULATING UNIT
BRANCH INSTRUCTION PROCESS UNIT
17
20
BRANCH HISTORY
IF_EAG
BRHIS_TIAR
19
18
INSTRUCTION COMPLETION PROCESS UNIT
EXECUTION INSTRUCTION PROCESS UNIT
W
U
X
TO OTHER INSTRUCTION PROCESS MECHANISMS

FIG. 5


BRHIS-RAM#0
IF_EAG<28>=0
BRHIS-RAM#1
IF_EAG<28>=1
IF_EAG<17:27>
21−2
21−1
LOW-ORDER 8 BYTES
HIGH-ORDER 8 BYTES
SEARCH RESULT OF BRANCH HISTORY

F I G. 6

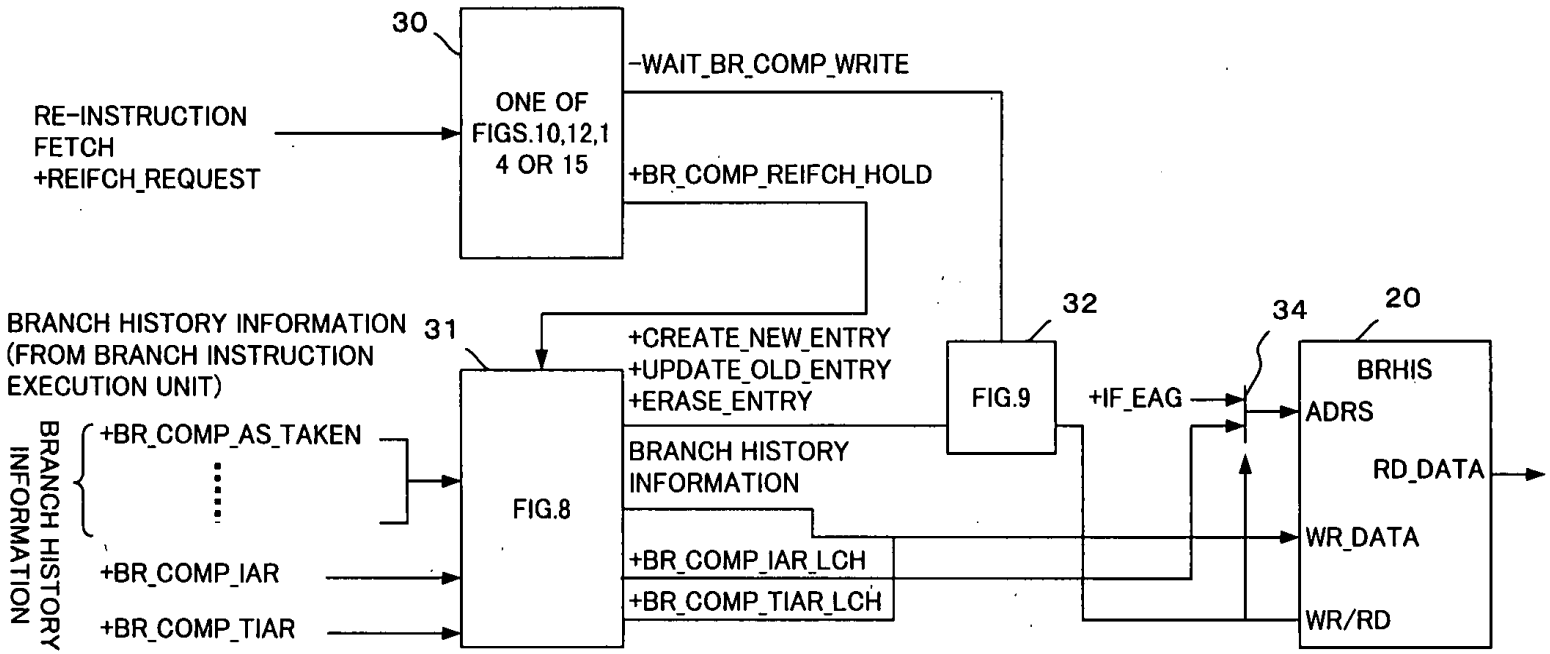

30
ONE OF FIGS.10,12,14 OR 15
RE-INSTRUCTION FETCH +REIFCH_REQUEST
-WAIT_BR_COMP_WRITE
+BR_COMP_REIFCH_HOLD
BRANCH HISTORY INFORMATION (FROM BRANCH INSTRUCTION EXECUTION UNIT)
31
BRANCH HISTORY INFORMATION
+BR_COMP_AS_TAKEN
+BR_COMP_IAR
+BR_COMP_TIAR
FIG.8
+CREATE_NEW_ENTRY
+UPDATE_OLD_ENTRY
+ERASE_ENTRY
BRANCH HISTORY INFORMATION
+BR_COMP_IAR_LCH
+BR_COMP_TIAR_LCH
32
FIG.9
34
+IF_EAG
20
BRHIS
ADRS
RD_DATA
WR_DATA
WR/RD

FIG. 7

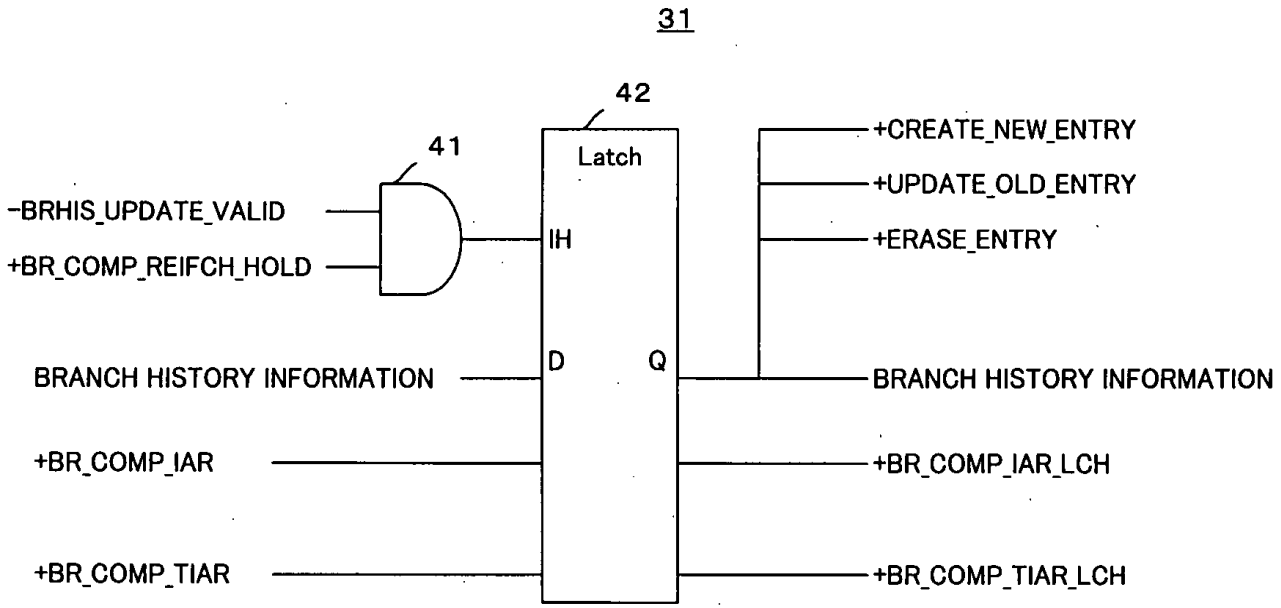


FIG. 8

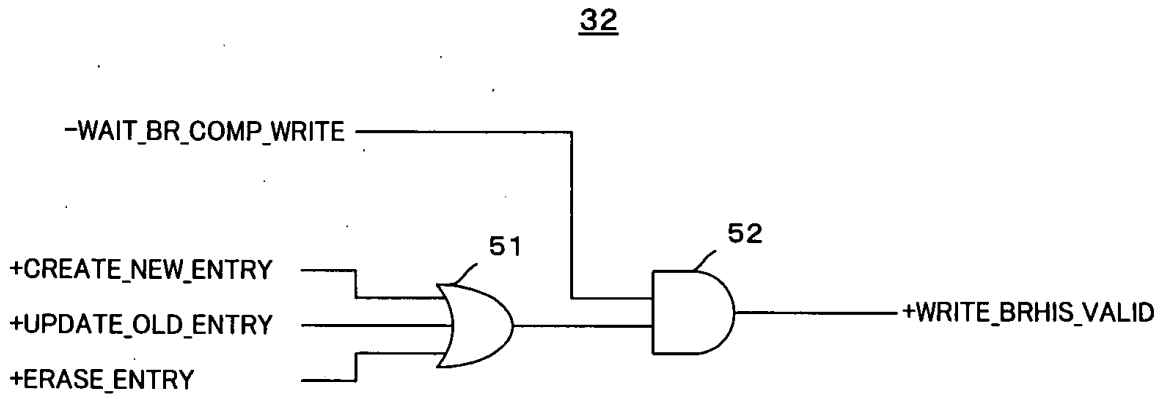


FIG. 9

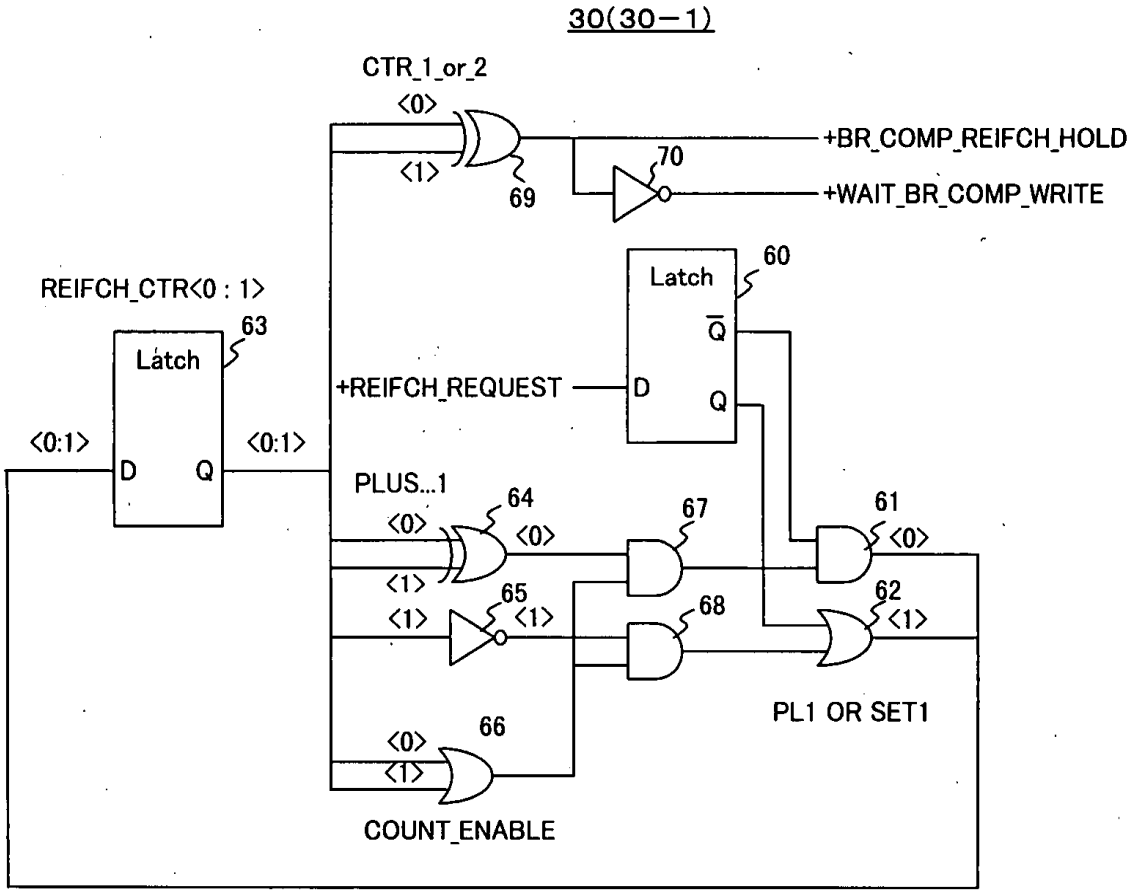

30(30−1)
CTR_1_or_2
<0>
<1>
69
70
+BR_COMP_REIFCH_HOLD
+WAIT_BR_COMP_WRITE
Latch
60
Q
D
Q
+REIFCH_REQUEST
REIFCH_CTR<0 : 1>
63
Latch
<0:1>
D
Q
<0:1>
PLUS...1
64
<0>
<1>
<0>
67
61
<0>
65
<1>
<1>
68
62
<1>
PL1 OR SET1
66
<0>
<1>
COUNT_ENABLE

FIG. 10

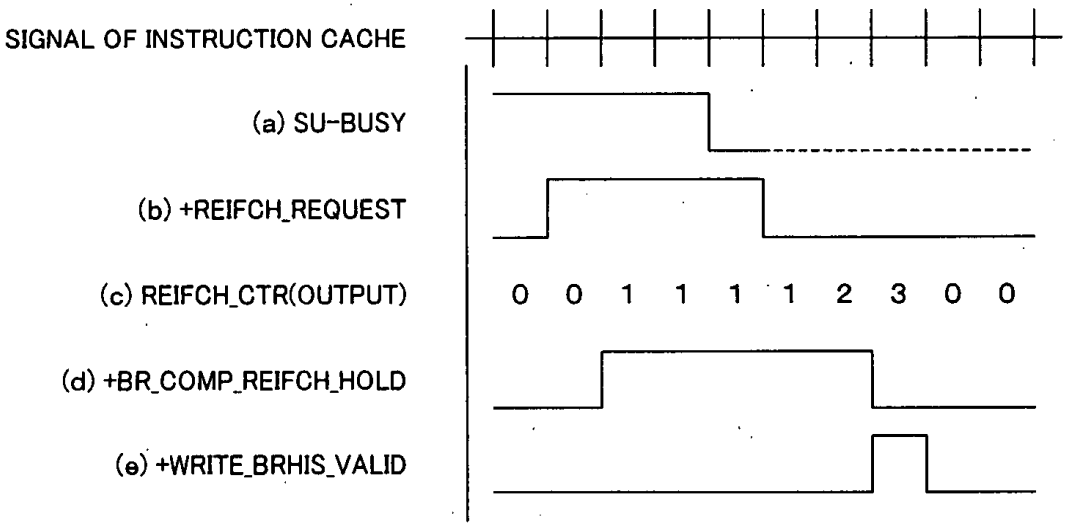


FIG. 11

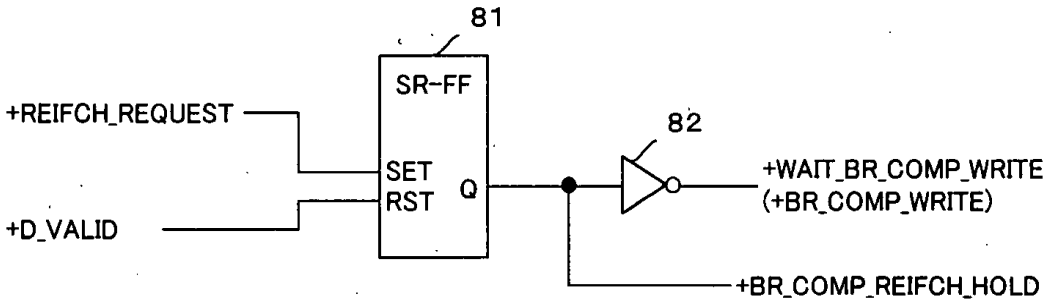

81
SR-FF
+REIFCH_REQUEST
SET
RST
Q
+D_VALID
82
+WAIT_BR_COMP_WRITE
(+BR_COMP_WRITE)
+BR_COMP_REIFCH_HOLD

FIG. 12

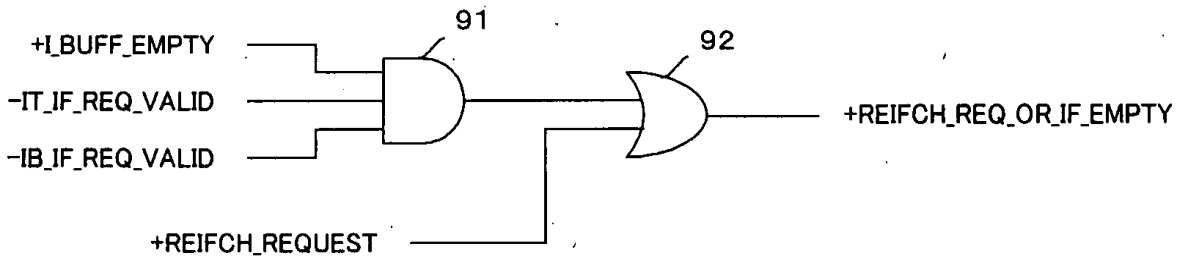


FIG. 13

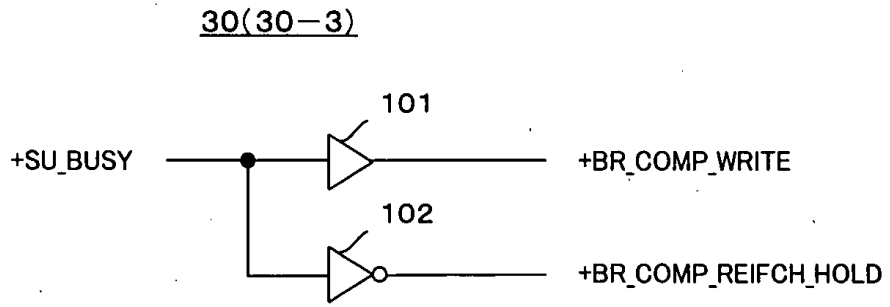


FIG. 14

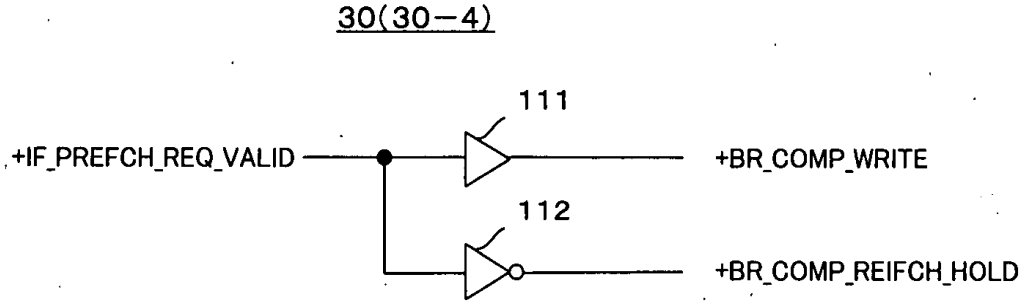


FIG. 15

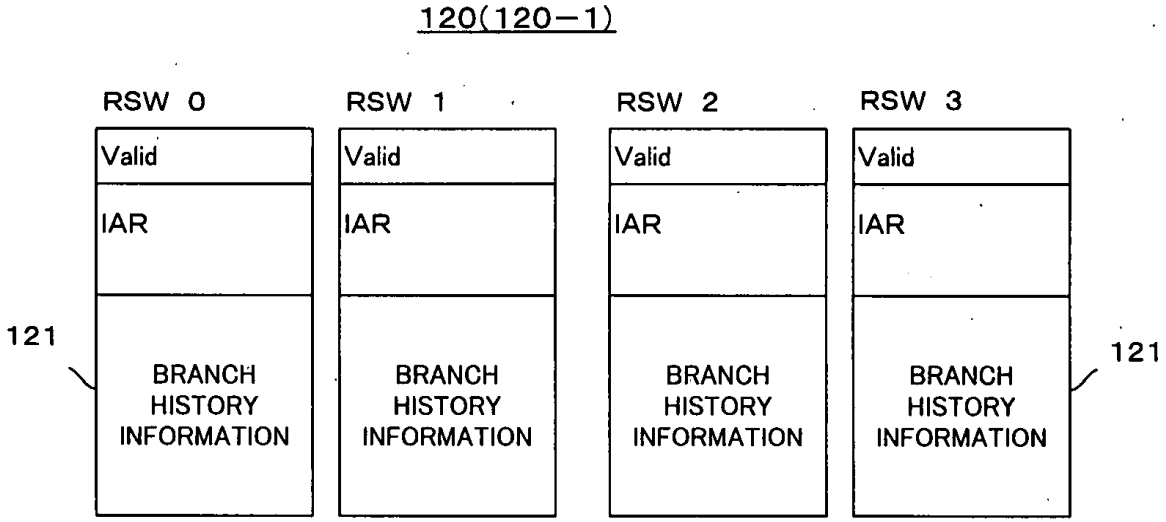


FIG. 16

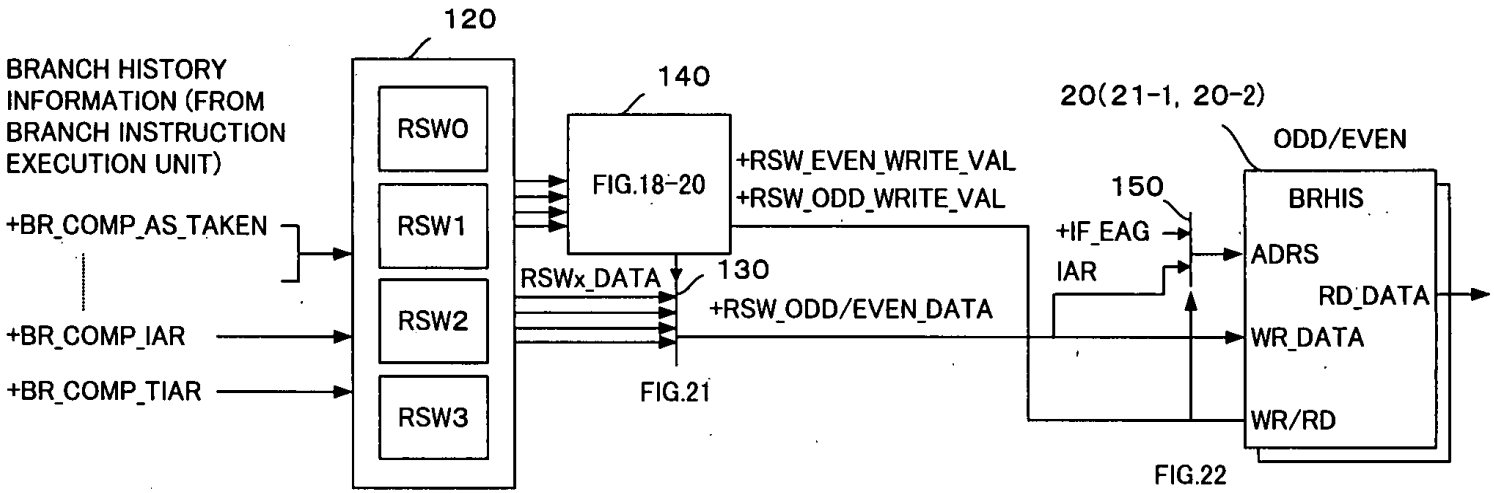

120
BRANCH HISTORY INFORMATION (FROM BRANCH INSTRUCTION EXECUTION UNIT)
+BR_COMP_AS_TAKEN
+BR_COMP_IAR
+BR_COMP_TIAR
RSW0
RSW1
RSW2
RSW3
140
FIG.18-20
+RSW_EVEN_WRITE_VAL
+RSW_ODD_WRITE_VAL
RSWx_DATA
130
+RSW_ODD/EVEN_DATA
FIG.21
20(21-1, 20-2)
ODD/EVEN
150
+IF_EAG
IAR
BRHIS
ADRS
RD_DATA
WR_DATA
WR/RD
FIG.22

FIG. 17

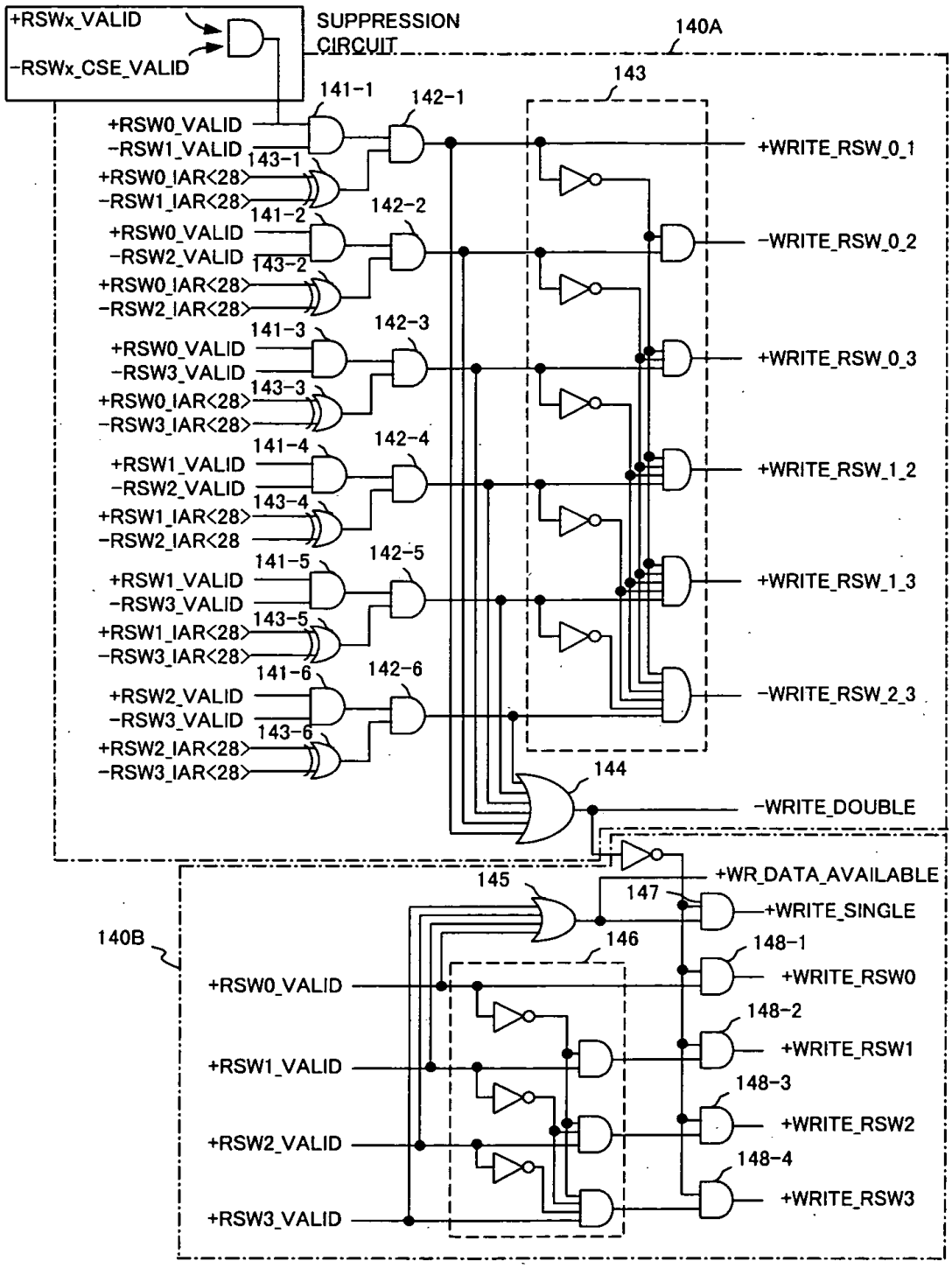


FIG. 18

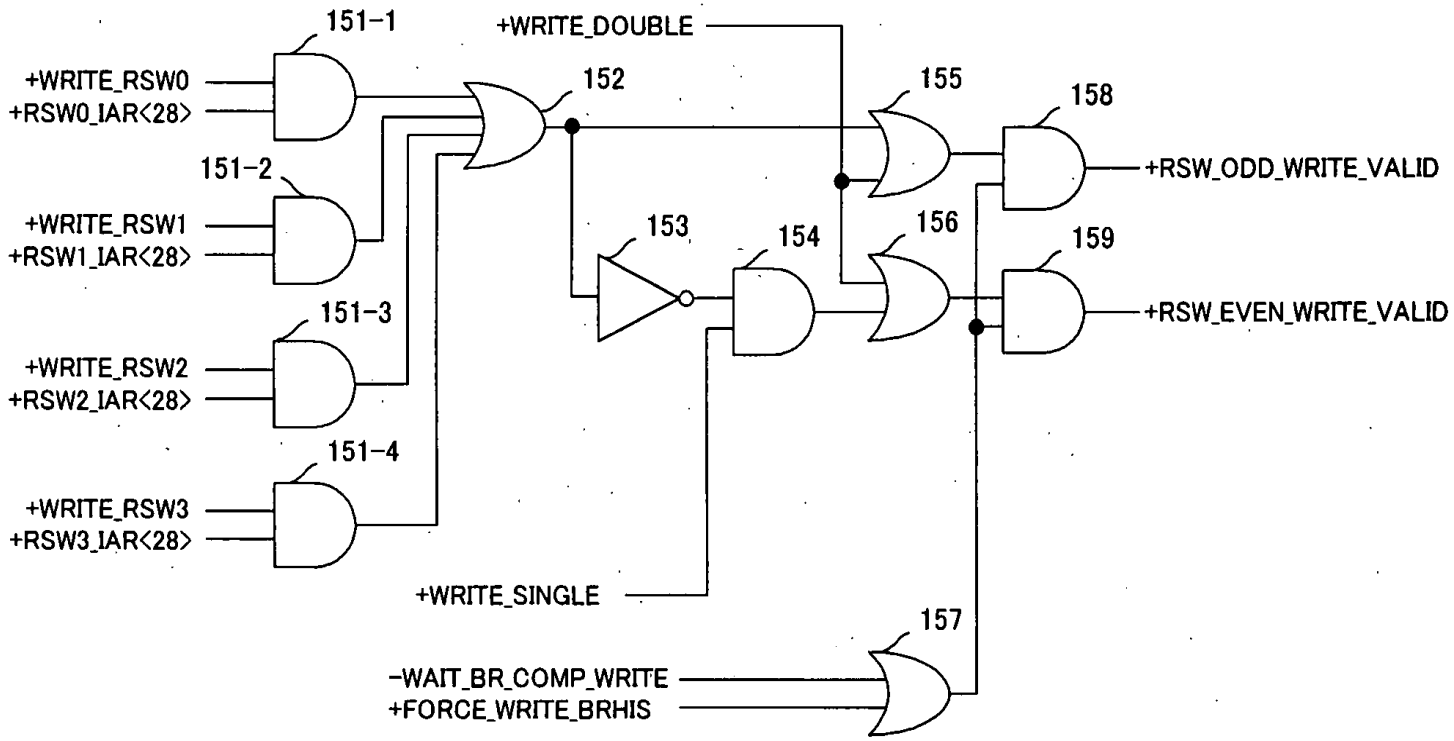

151-1
+WRITE_RSW0
+RSW0_IAR<28>
151-2
+WRITE_RSW1
+RSW1_IAR<28>
151-3
+WRITE_RSW2
+RSW2_IAR<28>
151-4
+WRITE_RSW3
+RSW3_IAR<28>
+WRITE_DOUBLE
152
153
154
155
156
157
158
159
+RSW_ODD_WRITE_VALID
+RSW_EVEN_WRITE_VALID
+WRITE_SINGLE
-WAIT_BR_COMP_WRITE
+FORCE_WRITE_BRHIS

FIG. 19

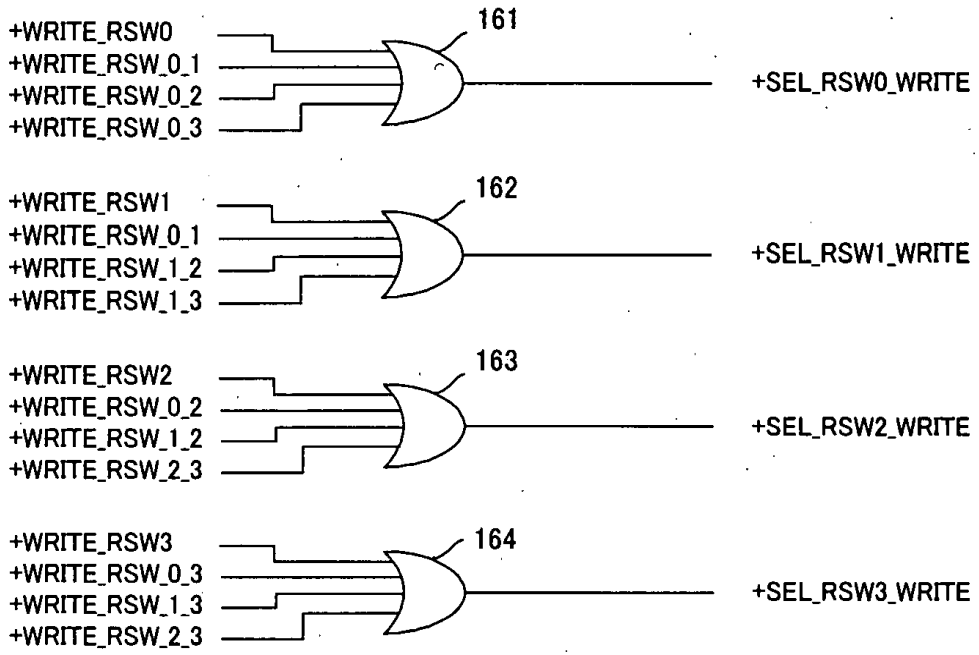


FIG. 20

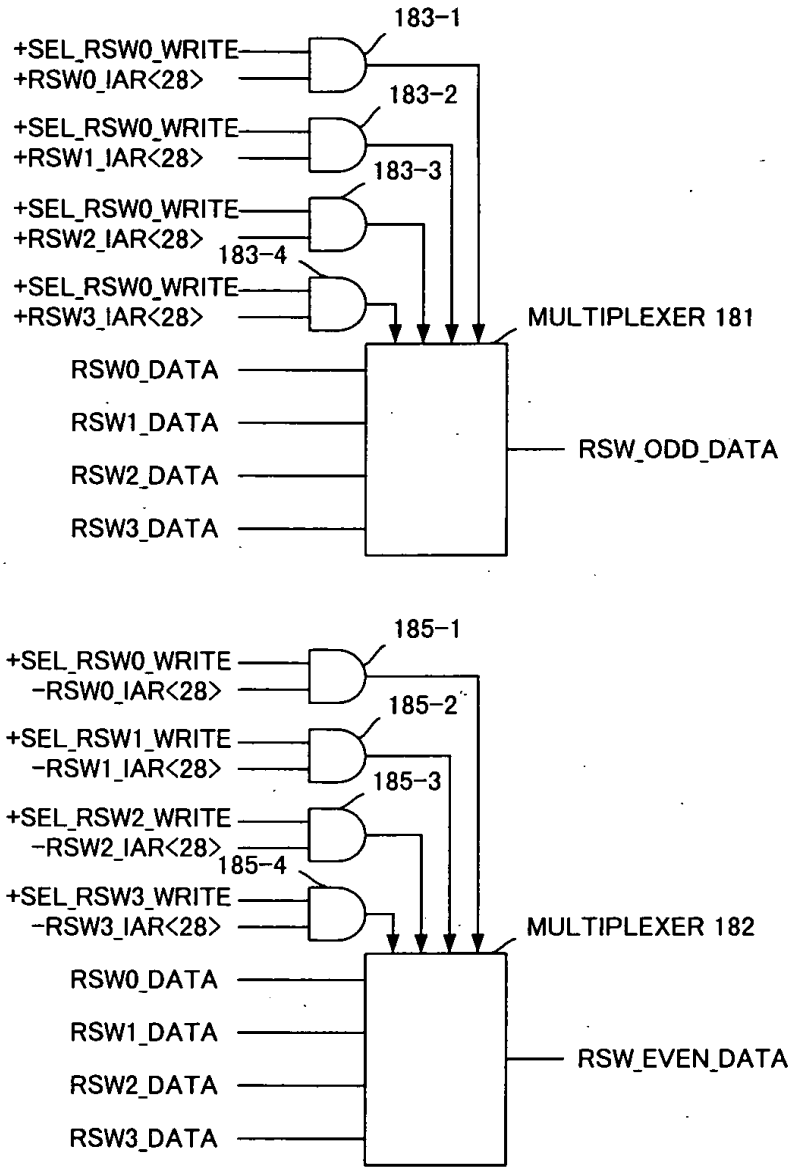


FIG. 21

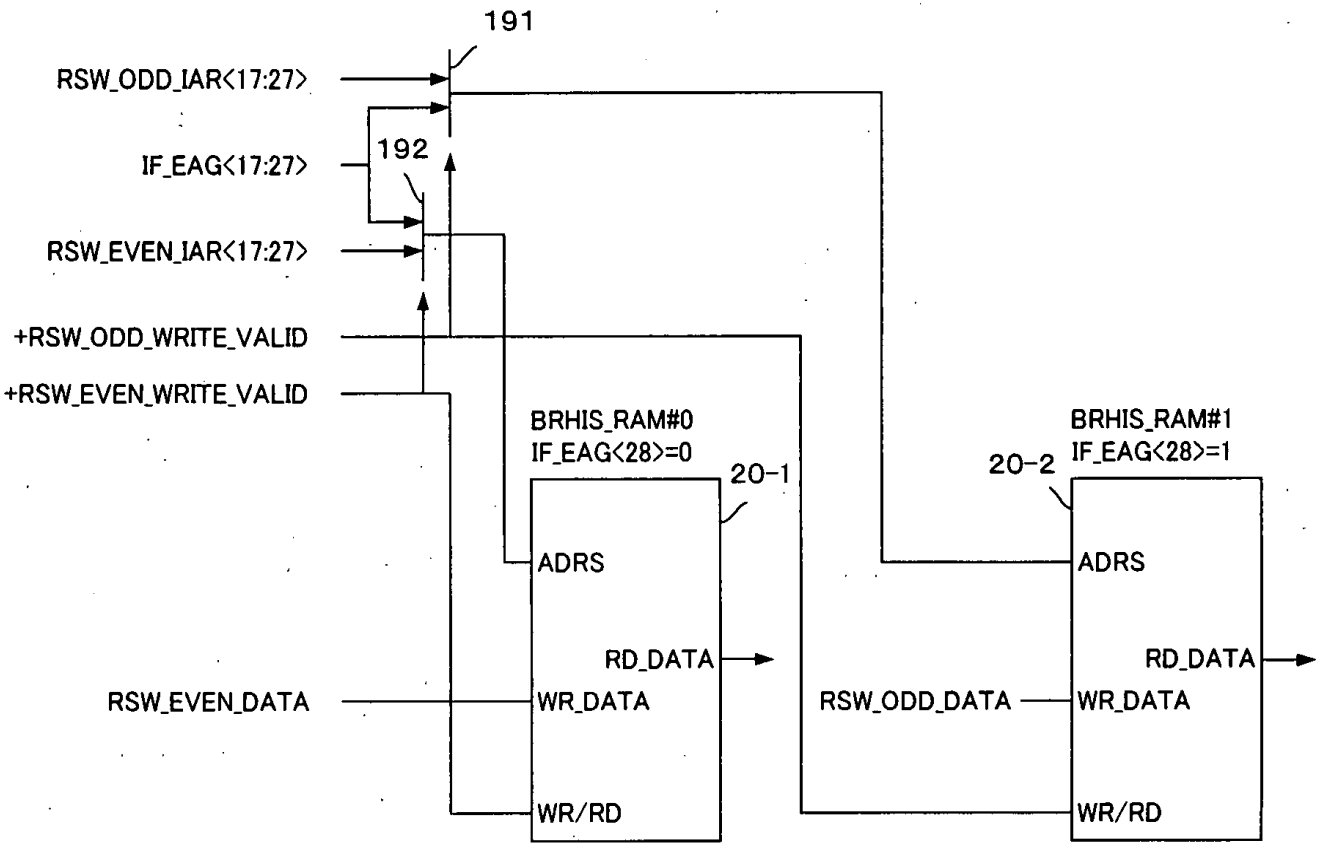


FIG. 22

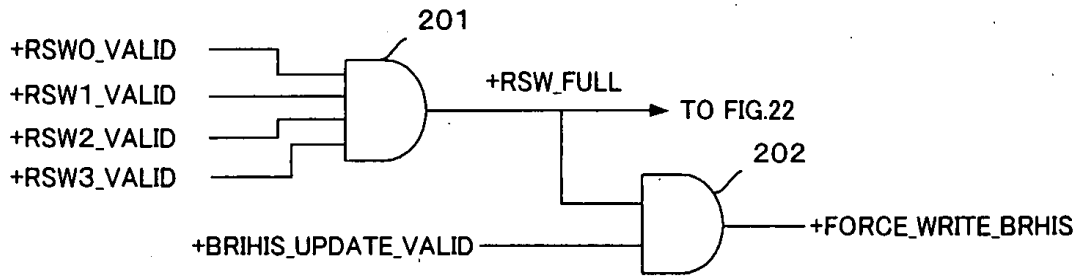


FIG. 23

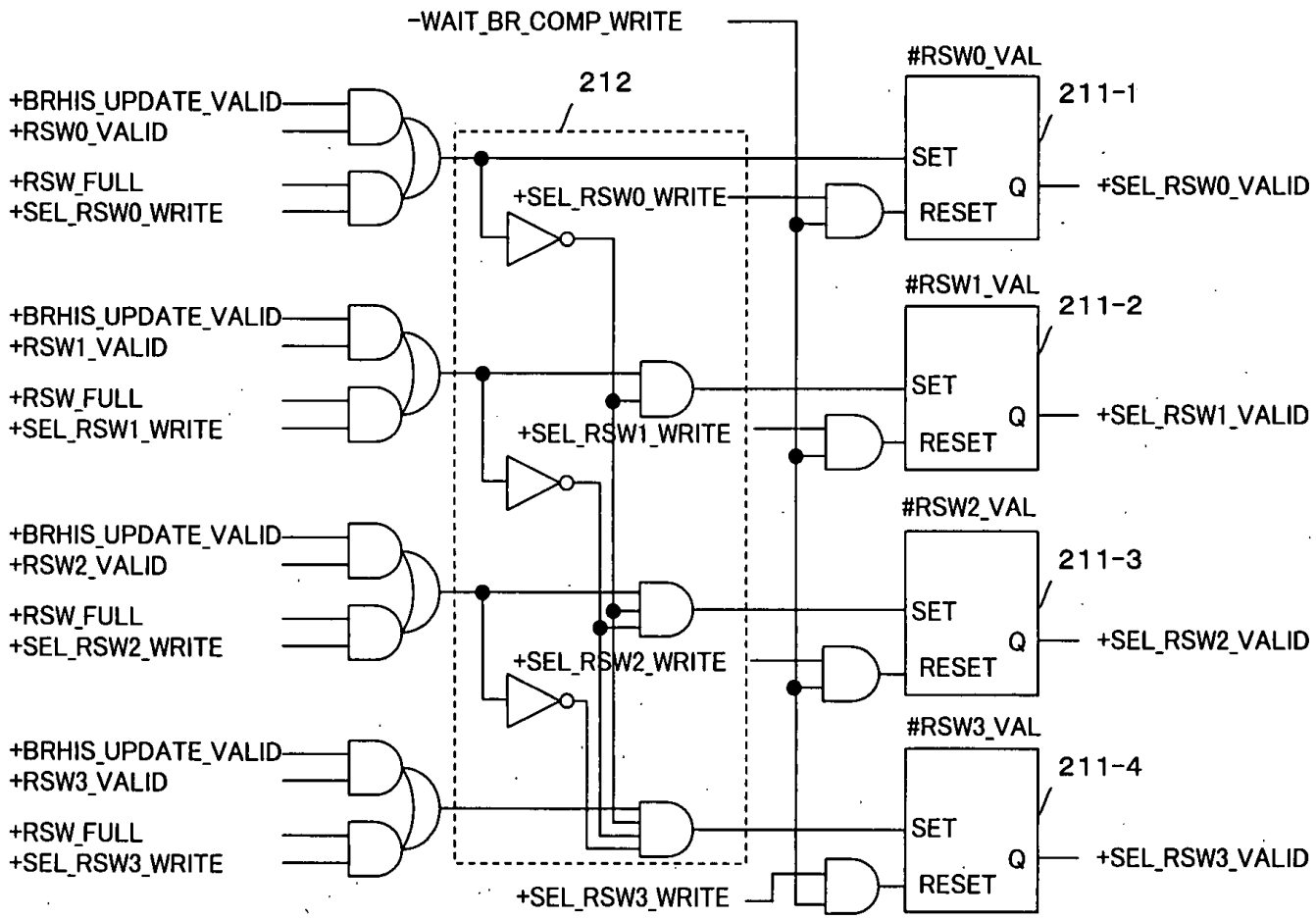


FIG. 24

120(120-2)

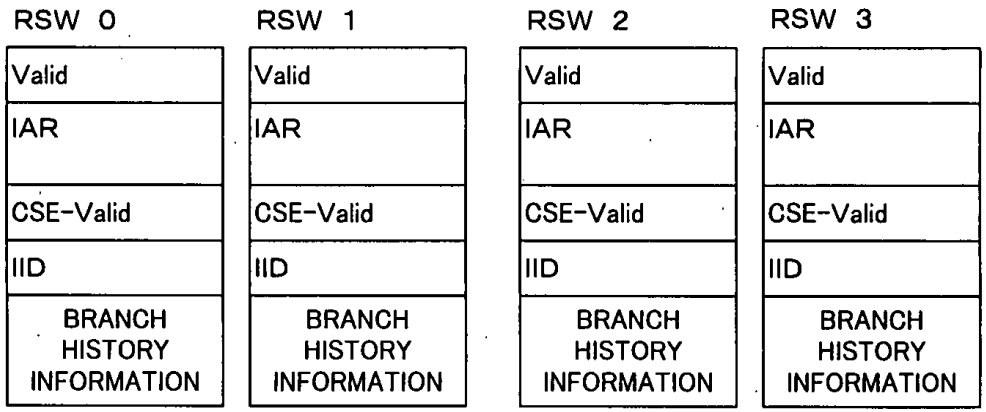


FIG. 25

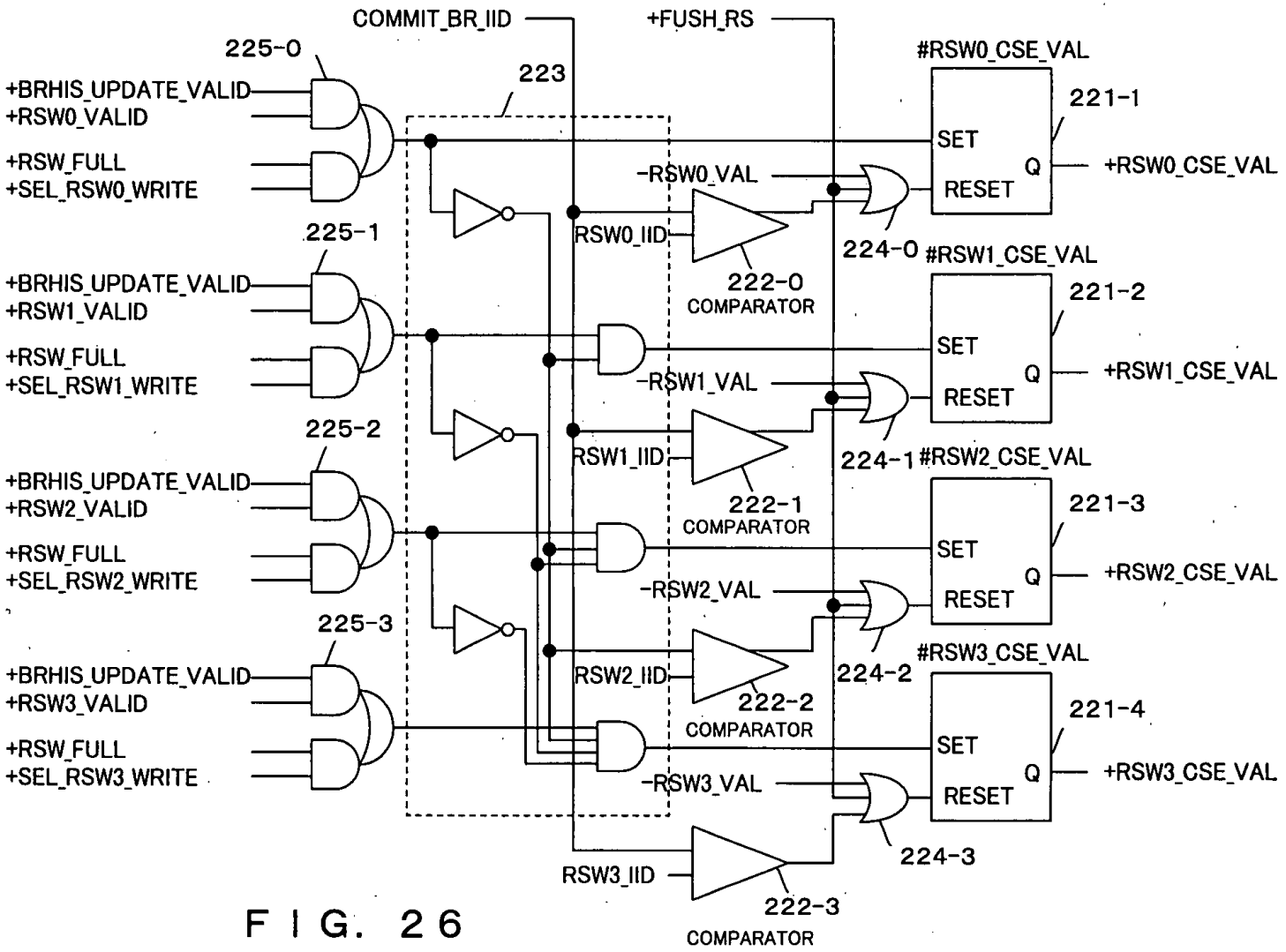

COMMIT_BR_IID
+FUSH_RS
225-0
223
+BRHIS_UPDATE_VALID
+RSW0_VALID
+RSW_FULL
+SEL_RSW0_WRITE
#RSW0_CSE_VAL
221-1
SET
Q
RESET
+RSW0_CSE_VAL
-RSW0_VAL
RSW0_IID
222-0
COMPARATOR
224-0
225-1
#RSW1_CSE_VAL
221-2
+BRHIS_UPDATE_VALID
+RSW1_VALID
+RSW_FULL
+SEL_RSW1_WRITE
-RSW1_VAL
RSW1_IID
222-1
COMPARATOR
224-1
+RSW1_CSE_VAL
225-2
#RSW2_CSE_VAL
221-3
+BRHIS_UPDATE_VALID
+RSW2_VALID
+RSW_FULL
+SEL_RSW2_WRITE
-RSW2_VAL
RSW2_IID
222-2
COMPARATOR
224-2
+RSW2_CSE_VAL
225-3
#RSW3_CSE_VAL
221-4
+BRHIS_UPDATE_VALID
+RSW3_VALID
+RSW_FULL
+SEL_RSW3_WRITE
-RSW3_VAL
RSW3_IID
222-3
COMPARATOR
224-3
+RSW3_CSE_VAL

FIG. 26

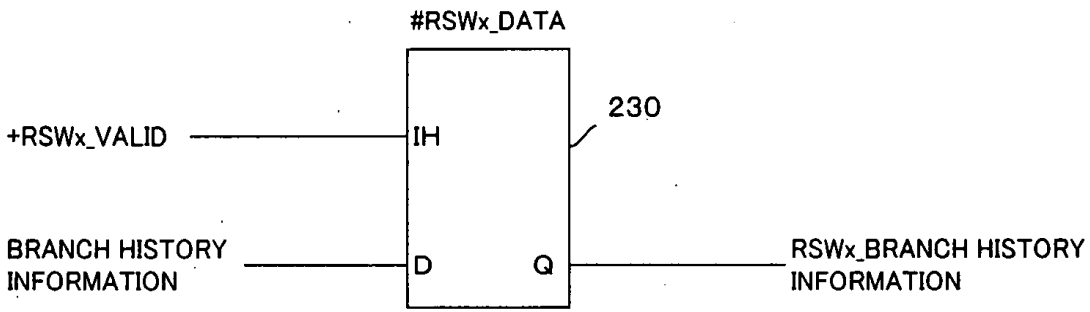
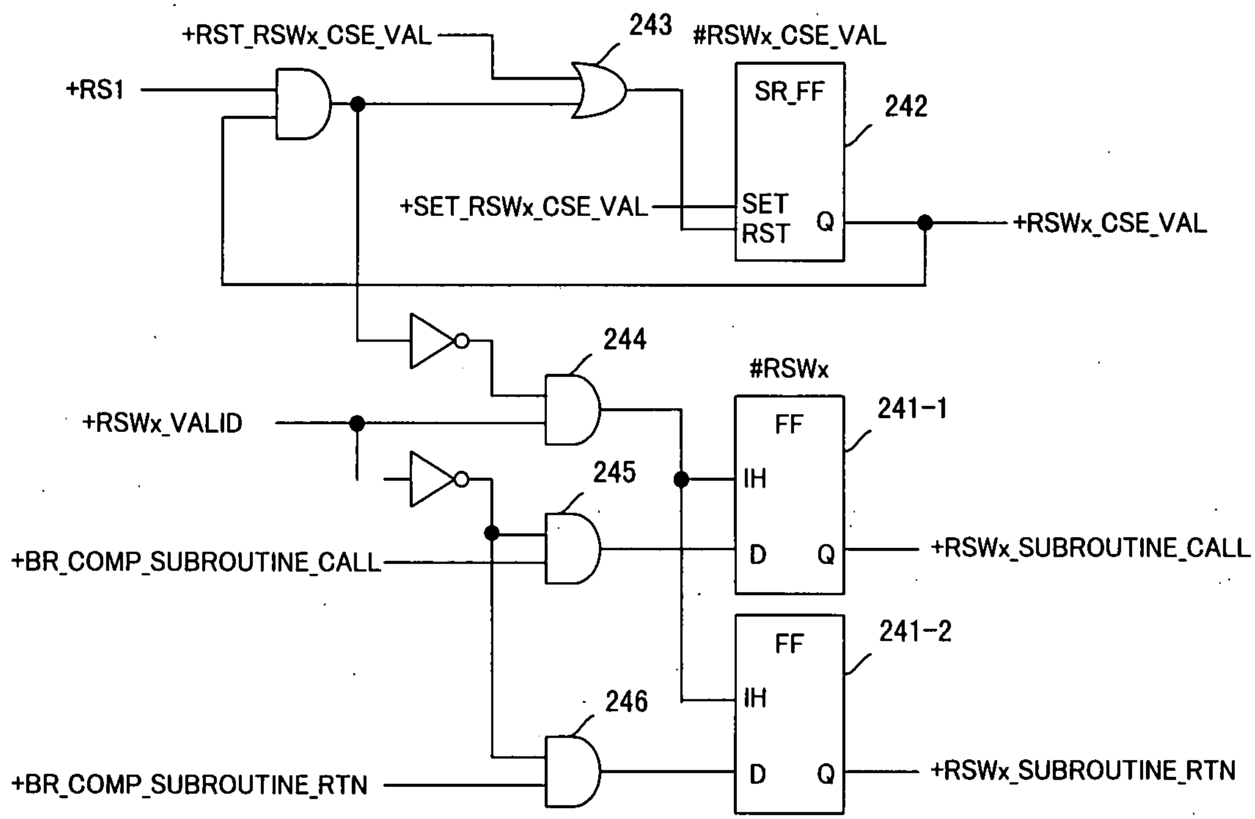


FIG. 27


+RST_RSWx_CSE_VAL
243
#RSWx_CSE_VAL
SR_FF
242
+RS1
+SET_RSWx_CSE_VAL
SET
RST
Q
+RSWx_CSE_VAL
244
#RSWx
FF
241-1
+RSWx_VALID
245
IH
+BR_COMP_SUBROUTINE_CALL
D
Q
+RSWx_SUBROUTINE_CALL
FF
241-2
246
IH
+BR_COMP_SUBROUTINE_RTN
D
Q
+RSWx_SUBROUTINE_RTN

F I G. 28

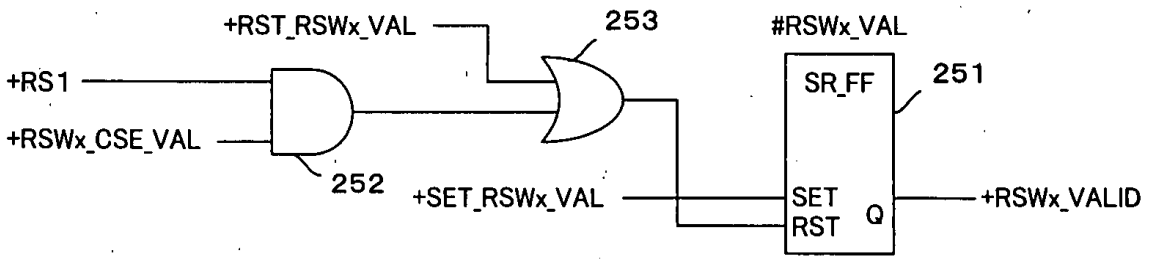


FIG. 29

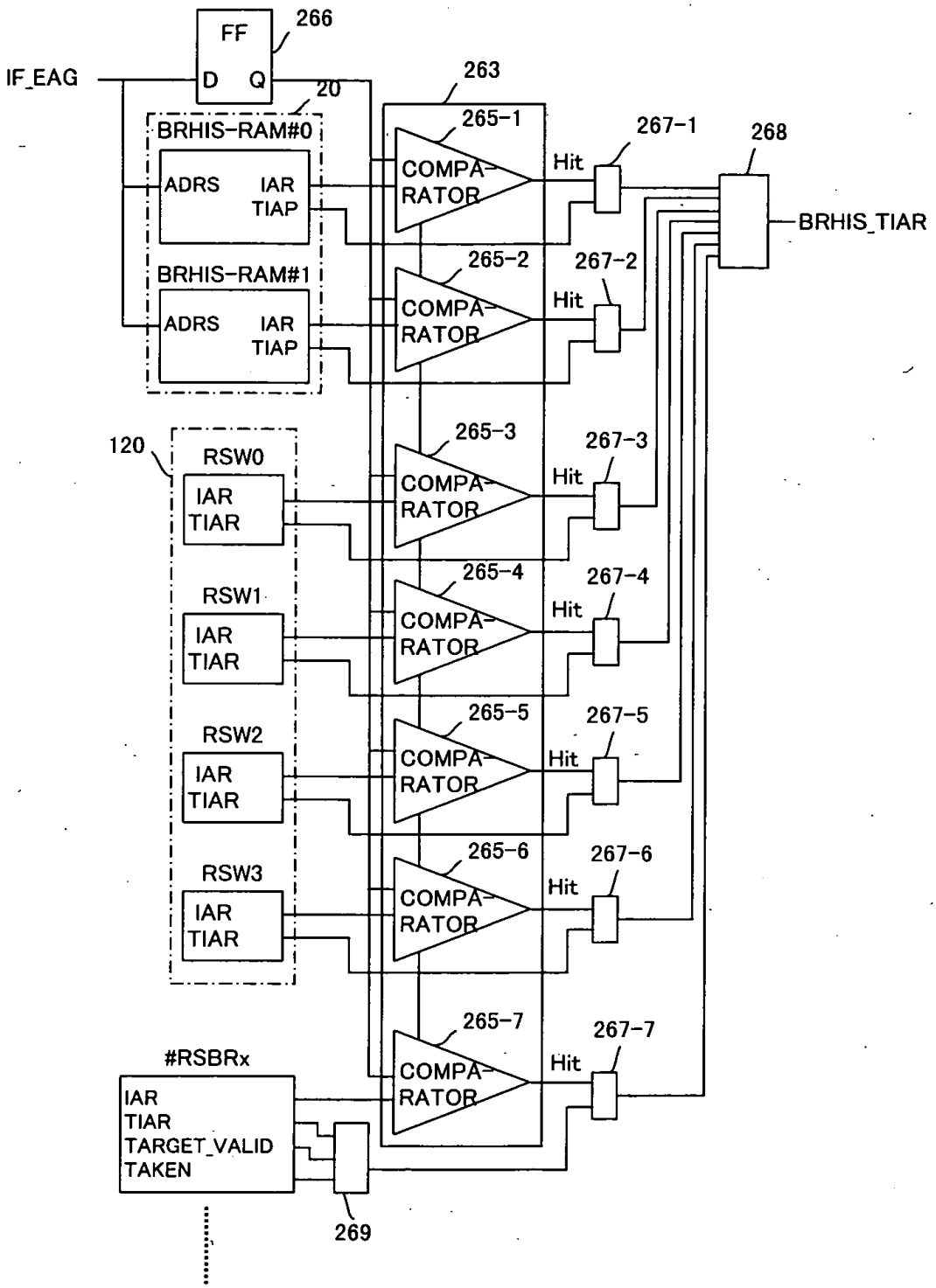


FIG. 30